WE CLAIM:

1. A method of forming a patterned structure in an integrated circuit at a semiconductor surface of a substrate, comprising the steps of:

forming a first layer over the surface;

applying a layer of photosensitive masking material over the first layer;

exposing the photosensitive masking material to light through a photomask having an elongated feature, the feature having a plurality of first sections along its length of a width at or greater than a critical photolithographic dimension, and having at least one second section disposed between adjacent ones of the first sections of the feature, the at least one second section having a width less than the critical photolithographic dimension;

after the exposing step, removing the photosensitive masking material from locations not corresponding to the location at which the patterned structure is to be formed; and

etching the first layer to form the patterned structure.

2. The method of claim 1, wherein the critical photolithographic dimension corresponds to a minimum line width that may be defined by the exposing and removing of the photosensitive masking material.

3. The method of claim 1, wherein the first layer comprises a conductive material.

4. The method of claim 3, further comprising:

after the etching step, doping locations of the surface adjacent the patterned structure.

5. The method of claim 1, wherein the first layer comprises an insulator material.

6. The method of claim 5, further comprising:

after the etching step, depositing a second layer overall, the second layer comprising a conductive material and extending into the etched portions of the first layer.

7. The method of claim 1, wherein each of the plurality of first sections extends for a selected length along the feature;

and wherein the at least one second section extends for a length along the feature that is less than about three times the selected length of the plurality of first sections.

8. The method of claim 1, wherein the at least one second section and its adjacent ones of the plurality of first sections have sides that are substantially parallel to the length of the elongated feature;

and wherein the elongated feature has edges, between the at least one second section and its adjacent ones of the plurality of first sections, that are substantially perpendicular to the sides of the at least one second section and its adjacent ones of the plurality of first sections.

9. The method of claim 8, wherein the elongated feature has a side that defines substantially a straight line segment.

10. The method of claim 1, wherein the at least one second section and its adjacent ones of the plurality of first sections have sides that are substantially parallel to the length of the elongated feature;

wherein the sides of the at least one second section and its adjacent ones of the plurality of first sections are separated by sloping portions of the elongated feature.

11. The method of claim 10, wherein the elongated feature has a side that defines substantially a straight line segment.

12. The method of claim 1, wherein the at least one second section and its adjacent ones of the plurality of first sections have sides that are substantially parallel to the length of the elongated feature;

and wherein opposing sides of the at least one second section and its adjacent ones of the plurality of first sections are substantially aligned with one another.

13. The method of claim 1, wherein the at least one second section and its adjacent ones of the plurality of first sections have sides that are substantially parallel to the length of the elongated feature;

and wherein opposing sides of the at least one second section and its adjacent ones of the plurality of first sections are staggered relative to one another.

14. A transistor formed at a semiconductor surface of a substrate, comprising:

a gate electrode extending along the surface for a length, the gate electrode having at least one second section disposed between adjacent ones of the first sections of the gate electrode, the at least one second section having a width that is narrower than the width of the adjacent ones of the first sections of the gate electrode; and

source and drain doped regions in the surface, and disposed on opposing sides of the gate electrode;

wherein the gate electrode is formed by a process comprising the steps of:

forming a conductive layer over the surface;

applying a layer of photosensitive masking material over the conductive layer;

exposing the photosensitive masking material to light through a photomask having an elongated feature, the feature having a plurality of first sections

along its length of a width at or greater than a critical photolithographic dimension, and having at least one second section disposed between adjacent ones of the first sections of the feature, the at least one second section having a width less than the critical photolithographic dimension, the first sections and at least one second section of the feature defining the first sections and at least one second section of the gate electrode;

after the exposing step, removing the photosensitive masking material from locations not corresponding to the location of the gate electrode; and

etching the conductive layer to form the gate electrode.

15. The transistor of claim 14, wherein the critical photolithographic dimension corresponds to a minimum line width that may be defined by the exposing and removing of the photosensitive masking material.

16. The transistor of claim 14, wherein the conductive material comprises polysilicon.

17. The transistor of claim 14, wherein each of the plurality of first sections extends for a selected length along the feature;

and wherein the at least one second section extends for a length along the feature that is less than about three times the selected length of the plurality of first sections.

18. The transistor of claim 14, wherein the at least one second section and its adjacent ones of the plurality of first sections have sides that are substantially parallel to the length of the elongated feature;

and wherein the elongated feature has edges, between the at least one second section and its adjacent ones of the plurality of first sections, that are substantially perpendicular to the sides of the at least one second section and its adjacent ones of the plurality of first sections.

19. The transistor of claim 18, wherein the elongated feature has a side that defines substantially a straight line segment.

20. The transistor of claim 14, wherein the at least one second section and its adjacent ones of the plurality of first sections have sides that are substantially parallel to the length of the elongated feature;

wherein the sides of the at least one second section and its adjacent ones of the plurality of first sections are separated by sloping portions of the elongated feature.

21. The transistor of claim 14, wherein the elongated feature has a side that defines substantially a straight line segment.

22. The transistor of claim 14, wherein the at least one second section and its adjacent ones of the plurality of first sections have sides that are substantially parallel to the length of the elongated feature;

and wherein opposing sides of the at least one second section and its adjacent ones of the plurality of first sections are substantially aligned with one another.

23. The transistor of claim 14, wherein the at least one second section and its adjacent ones of the plurality of first sections have sides that are substantially parallel to the length of the elongated feature;

and wherein opposing sides of the at least one second section and its adjacent ones of the plurality of first sections are staggered relative to one another.

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